

Sub B2

METHOD AND APPARATUS FOR JUMP DELAY SLOT CONTROL IN A PIPELINED PROCESSOR

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Abstract of the Disclosure

An improved method and apparatus for implementing instructions in a pipelined central processing unit (CPU) or user-customizable microprocessor. In a first aspect of the 10 invention, an improved method of controlling branching and the execution of instructions within the pipeline is disclosed. In one embodiment, the method comprises defining three discrete delay slot modes within program jump instructions; these delay slot modes specify the execution of subsequent instructions or the stalling of the pipeline as desired by the programmer. In a second aspect of the invention, a method of synthesizing a processor 15 design incorporating the aforementioned modes is disclosed. Exemplary gate logic synthesized using the aforementioned methods, and a computer system capable of implementing these methods, are also described.

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